Pimpri Chinchwad Education Trust's

PIMPRI CHINCHWAD COLLEGE OF ENGINEERING

SECTOR NO. 26, PRADHIKARAN, NIGDI, PUNE 411044

An Autonomous Institute Approved by AICTE and Affiliated to SPPU, Pune

DEPARTMENT OF ELECTRONICS AND TELECOMMUNICATION ENGINEERING

Curriculum Structure and Syllabus

Honors in

Semiconductor Technology

(Regulations 2023)

Effective from Academic Year 2026-27

(Updated with minor Changes)

Institute Vision

To be one of the top 100 Engineering Institutes of India in coming five years by offering exemplarily Ethical, Sustainable and Value Added Quality Education through a matching ecosystem for building successful careers.

Institute Mission

1. Serving the needs of the society at large through establishment of a state-of-art Engineering Institute.
2. Imparting right Attitude, Skills, Knowledge for self-sustenance through Quality Education.
3. Creating globally competent and Sensible engineers, researchers and entrepreneurs with an ability to think and act independently in demanding situations.

EOMS Policy

"We at PCCOE are committed to offer exemplarily Ethical, Sustainable and Value Added Quality Education to satisfy the applicable requirements, needs and expectations of the Students and Stakeholders.

We shall strive for technical development of students by creating globally competent and sensible engineers, researchers and entrepreneurs through Quality Education.

We are committed for Institute's social responsibilities and managing Intellectual property.

We shall achieve this by establishing and strengthening state-of-the-art Engineering Institute through continual improvement in effective implementation of Educational Organizations Management Systems (EOMS)."

Course Approval Summary

Board of Studies - Department of E&TC Engineering

Sr. No.	Name of the Course	Course Code	Page number	Signature and stamp of BoS chairman
1	Digital Integrated Circuits	BET25HN11	10	
2	Digital Integrated Circuits Lab	BET25HN12	13	
3	Analog Circuits and Advance MOS Devices	BET26HN11	15	
4	Analog Circuits and Advance MOS Devices Lab	BET26HN12	17	
5	VLSI Physical Design and fabrication techniques	BET27HN11/ BET28HN12	19	
6	Project	BET28HN11/ BET27HN13	21	

Approved by Academic Council:

Chairman, Academic Council
Pimpri Chinchwad College of Engineering,Pune

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Preface

With rapid evolution in technologies and an increasing demand for latest innovation in products and services, the semiconductor manufacturing industry is expected to rise. From smart phones to cars, manufacturers and the semiconductor industry are ramping up to meet the world's seemingly insatiable demand for chips. Semiconductor chips have become essential to everyday lives and that dependence is predicted to grow to cater industry demands. Emerging markets and technologies such as AI, robotic process automation and 5G connectivity are also fueling the growth of the semiconductor industry. From a recruitment perspective, several new jobs are being created across sectors and across specializations.
For Honors degree program, student has to earn additional 20 credits in emerging area of one's own domain.

Objectives of Honors Degree

1. To enable students to pursue allied academic interest in contemporary areas.
2. To provide effective yet flexible options for students to achieve basic to intermediate level competence in the contemporary area.
3. To enhance the employability skills with different combinations of competencies and flavors.
4. To provide an academic mechanism for fulfilling demand of specialized areas from industries for higher order skill jobs.
5. To provide a strong foundation to students aiming to pursue research/ higher studies in the contemporary field of study.

Semiconductor Technology

Objectives:

1. Introduce students to manufacturing processes involved in semiconductor industry
2. Explain semiconductor devices with its practical applications
3. Provide knowledge of CMOS technology and need of advanced CMOS technology to cater performance requirement
4. Give exposure to software EDA tools used in semiconductor industry

Outcomes: After completion of this program, students will be able to:

1. Analyze the performance of the semiconductor devices and circuits
2. Evaluate the performance of the MOSFET and multigate devices in nanometer region
3. Design combinational and sequential logic using CMOS and evaluate their performance.
4. Describe the short channels effect and the need of change of technology paradigm from CMOS to Advanced CMOS
5. Explain concepts of VLSI physical design and manufacturing processes involved in semiconductor industry

Curriculum Structure

Curriculum structure- Scheme-A

Sem-ester	Course Code	Course Name	Teaching Scheme					Evaluation Scheme						
			L	P	T	Hrs	CR	FA1	FA2	SA	TW	PR	OR	Total
V	BET25HN11	Digital Integrated Circuits	4	-	-	4	4	20	20	60	-	-	-	100
	BET25HN12	Digital Integrated Circuits Lab	-	2	-	2	1	-	-	-	25	-	25	50
VI	BET26HN11	Analog Circuits and Advance MOS Devices	4	-	-	4	4	20	20	60	-	-	-	100
	BET26HN12	Analog Circuits and Advance MOS Devices Lab	-	2	-	2	1	-	-	-	25	-	25	50
VII	BET27HN11	VLSI Physical Design and fabrication techniques	4	-	-	4	4	20	20	60	-	-	-	100
VIII	BET28HN11	Project	-	8		8	4	-	-	-	100		50	150
Total			**12**	**12**		**24**	**18**	**60**	**60**	**180**	**150**	**-**	**100**	**550**

Abbreviations:
1 Lecture hour = 1 Credit 2 Lab Hours = 1 Credit 1 Tutorial Hour = 1 Credit Abbreviations are: L-Lecture, P-Practical, T-Tutorial, H- Hours, FA-Formative Assessment, SA-Summative assessment TW –Term work, OR – Oral, CR- Credits

Curriculum structure- Scheme-B

Sem-ester	Course Code	Course Name	Teaching Scheme					Evaluation Scheme						
			L	P	T	Hrs	CR	FA1	FA2	SA	TW	PR	OR	Total
V	BET25HN11	Digital Integrated Circuits	4	-	-	4	4	20	20	60	-	-	-	100
	BET25HN12	Digital Integrated Circuits Lab	-	2	-	2	1	-	-	-	25	-	25	50
VI	BET26HN11	Analog Circuits and Advance MOS Devices	4	-	-	4	4	20	20	60	-	-	-	100
	BET26HN12	Analog Circuits and Advance MOS Devices Lab	-	2	-	2	1	-	-	-	25	-	25	50
VII	BET27HN13	Project	-	8		8	4	-	-	-	100		50	150
VIII	BET28HN12	VLSI Physical Design and fabrication techniques	4	-	-	4	4	20	20	60	-	-	-	100
Total			**12**	**12**		**24**	**18**	**60**	**60**	**180**	**150**	**-**	**100**	**550**

Course Syllabus
Semester - V

Program:	B. Tech. (E&TC-Honors)					Semester:	V
Course:	Digital Integrated Circuits					Code:	BET25HN11
Teaching Scheme (Hrs./Week)				Evaluation Scheme and Marks			
Credit	Lecture	Practical	Practical	FA		SA	Total
				FA1	FA2		
4	4	-	-	20	20	60	100

Prior Knowledge of:
Basics of semiconductor Physics, Digital Electronics is essential.

Course Objectives:

1. To emphasize on fundamental principles of MOSFET
2. To understand short channel effects in MOSFET in nanometer region
3. To focus on the design combinational and sequential logic gates using CMOS and its related timing issues

Course Outcomes:

After the completion of the course, the students will be able to:

1. Describe Working principle of MOSFET Device
2. Explain short channel effects in MOSFET in nanometer regime
3. Analyze CMOS inverter performance with respect to technology scaling in nanometer region
4. Design combinational and sequential logic gates using CMOS
5. Describe timing issues and clock distribution techniques in digital circuits
6. Design Arithmatic building blocks

Detailed Syllabus:

Unit	Description	Duration
1.	MOSFET Device: MOSFET Structure and Operation, MOSFET: I-V Characteristics MOS transistor under static condition, Dynamic behavior, MOS structure capacitances, Actual MOS transistor-some secondary effects, SPICE models.	11
2.	MOSFET in nanometer: Scaling and its impact, Short channel effects, Drain induced barrier lowering, sub-threshold leakage, punch through effect, hot carrier effect	9
3.	**Circuit Perspective**: CMOS Inverter, Performance of CMOS Inverter,Power,Energy, Energy-Delay, Technology Scaling and its Impact on the Inverter Metrics	11
4.	DESIGNING COMBINATIONAL & SEQUENTIAL LOGIC GATES In CMOS: Static CMOS Design, Dynamic CMOS Design, Power Consumption in CMOS Gates,Static Latches and Registers, Dynamic Latches and Registers	9
5.	TIMING ISSUES IN DIGITAL CIRCUITS: Introduction, Synchronous Timing basics, Clock Skew and Jitter, Clock distribution techniques, Clock Generation and Synchronization.	11
6.	Designing Arithmatic building blocks: Adder, Multiplier, Shifter, Power and Speed tradeoff in datapath structure	9
	Total	60

Text Books:

1. Jan M Rabaey, Digital Integrated Circuits, 2nd Edition, Pearson Education, 2003.
2. Sung-Mo Kang, CMOS Digital Integrated Circuits, 3rd Edition, McGraw-Hill, 2003.

Reference Books:

1. Neil H.E.Weste and Kamran Eshraghian, Principles of CMOS VLSI Design, A System Perspective, Pearson Education, India. 4. Ken Martin, Digital Integrated Circuits, Oxford Press.
2. CMOS Circuit Design, Layout and simulation: J. Baker, D.E. Boyce., IEEE press.
3. Semiconductor physics and Devices, Donald Neamen, McGraw-Hill, 3rd edition.

Program: B. Tech. (E&TC-Honors)				Semester:			VI
Course: Digital Integrated Circuits Lab				Code:			BET25HN12
Teaching Scheme (Hrs./Week)				Evaluation Scheme and Marks			
Credit	**Lecture**	**Practical**	**Tutorial**	**TW**	**OR**	**PR**	**Total**
01	--	02	-	25	25	--	50

Prior knowledge of:
Analog circuits and semiconductor devices

Objectives:
To design and analyze performance of combinational and sequential CMOS circuits

Outcomes: At the end of Laboratory work, the students will be able to:
CO 1: Design CMOS Circuits such as inverter and analyze its characteristics
CO 2: Design logic gates using different logic design styles to verify their performance CO 3: Design and Simulate Combinational circuits using EDA tool.
CO4 : Design and Simulate sequential circuits using EDA tool

Detailed Syllabus:

Expt. No.	List of Experiments
1	Design and Simulation of CMOS Inverter to study the transfer Characteristics by varying the design constraints using EDA Tools
2	Design and Simulation of logic gates using various logic styles and compare its performance
3	Develop HDL model, Simulate and Synthesize 32-bit Parallel adder using 8-bit adder module
4	Design and Simulate 32-bit Shift register using 8-bit Shift register module

Reference Books:

1. Samir Palnitkar, Verilog HDL, 2nd Edition, Pearson Education, 2003.
2. Douglas Perry, VHDL: Programming by Example, 2017

Course Syllabus
Semester - VI

Program:	B.Tech.(E&TC) - B. Tech. (E&TC-Honors)					Semester:	VI
Course:	Analog Circuits and Advance MOS Devices					Code:	BET26HN11
	Teaching Scheme (Hrs./Week)			Evaluation Scheme and Marks			
Credit	Lecture	Practical	Tutorial	FA		SA	Total
				FA1	FA2		
4	4	-	-	20	20	60	100

Prior Knowledge of: Basic knowledge of Analog Electronics and CMOS Devices.

Course Objectives:

To acquaint the students with basic CMOS analog building blocks and analogsub-system design. To make the students understand challenges with MOSFET in nanometer regime

To interpret the performance parameters and challenges of multi-gate devices

Course Outcomes:

After the completion of the course, the students should be able to:

CO1: Understand the MOSFET models and its various important parameters

CO2: Illustrate the operation of MOS current mirror and single stage amplifier

CO3: Analyze the performance parameter of Op-amp and differential amplifier.

CO4: Determine the MOSFET operational challenges in the nanometer region

CO5: Analyze the advantages and challenges in multi-gatedevices.

CO6: Compare various performance parameters of MOSFET and multi-gate devices

Detailed Syllabus:

Unit	Description	Duration
1.	Necessity and advantages of CMOS Analog Circuits, Overview of MOS amplifiers and their analysis; analysis of MOS circuits using square law; frequency response, bandwidth enhancement;	11
2.	Analog building blocks: MOS current mirror, cascade current mirrors, BW analysis and output impedance of CM, Single stage amplifier (SSA) configurations, cascode stage, Transconductance amplifier, frequency response.	9
3.	Differential amplifiers with MOS Loads, device mismatch effects, frequency response of differential amplifiers. Op-amp: Performance parameters, one & two-stage Op-amps, pole-zero compensation, gain boosting, active compensation, input range, slew rate, noise in op-amp.	11
4.	Advanced MOSFET: Silicon-On-Insulator (SOI) MOSFETs: Fully Depleted (FD) SOI, Partially Depleted (PD) SOI, Junction Less SOI	9
5.	MOSFET, multi-gate transistors: - single gate – double gate – triple gate – surround gate, quantum effects- advantages and challenges	11
6.	Digital circuits design, impact of device performance on digital circuits, leakage performance trade off, multi-VT devices and circuits.	9
	Total	60

Text Books:

1. Design of Analog CMOS Integrated Circuits, Behzad Razavi, McGraw Hill Indian, 2nd Edition (2017)
2. Wolf, W., “Modern VLSI Design System on Silicon”, 2nd Ed., Pearson Education
3. J P Colinge, “FINFETs and other multi-gate transistors”, Springer – Series on integrated circuits and systems, 2008.

Reference Books:

1. CMOS Circuit Design: Layout and Simulation, R. Jacob Baker, Wiley IEEE Press, 3rd Edition (2010)
2. CMOS Analog Circuit Design, E. Allen & Douglas R. Holberg, Oxford Press Int. Edition, 3rd Edition (2012)
3. Jean- PierrieColinge, Silicon-on-insulator Technology: Materials to VLSI, Kluwer Academicpublishers' group.
4. Sandip Kundu, Aswin Sreedhar, "Nanoscale CMOS VLSI Circuits: Designfor Manufacturability" McGraw Hill, 2010

Program:	B. Tech. (E&TC-Honors)	Semester: VI
Course:	Analog Circuits and Advance MOS Devices Lab	Code: BET26HN12

	Teaching Scheme (Hrs./Week)			Evaluation scheme and Marks			
Credit	**Lecture**	**Practical**	**Tutorial**	**TW**	**OR**	**PR**	**Total**
01	--	02	-	25	25	--	50

Prior knowledge of:
Analog circuits and semiconductor devices

Objectives:
To analyze performance parameters of analog circuits
To measure performance parameters of MOSFET and advanced CMOS devices with technology scaling

Outcomes: At the end of Laboratory work, the students will be able to: CO 1: Measure various performance parameters of analog circuits.
CO 2: perform transfer characteristics of MOSFET devices
CO 3: Analyze the impact of technology scaling on MOSFET and Advanced CMOS devices.

Detailed Syllabus:

Expt. No.	List of Experiments
1	Design and simulation of Single Stage Amplifier and transconductance plot
2	Design and simulation of Common Source Amplifier
3	Design and simulation of Single Stage Amplifier with different load
4	Implementation of CMOS Inverter. Obtain & Plot Its Transfer Characteristics, Determine Noise Margins and Measure Propagation Delay.
5	Design SRAM cell using MOSFET and analyze impact of short channel effects on its performance in nanometer region
6	Implement and analyze I-V characteristics of FinFET using Microwind

Reference Books:

1. R. Jacob Baker, CMOS: circuit Design, Layout and Simulation, Wiley, 2009
2. Douglas R. Holberg, Phillip E. Allen, CMOS Analog Design, 3rd Edition, Oxford University Press, 2013.
3. Brajesh Kumar Kaushik, Nanoscale Devices: Physics, Modeling, and Their Application, CRC Press, 2018

Course Syllabus
Semester – VII/VIII

Program:	B. Tech. (E&TC) -Honors In Semiconductor Technology	Semester:	VI
Course:	VLSI Physical Design and Fabrication Techniques	Code:	BET27HN11/ BET28HN12

Teaching Scheme				Evaluation Scheme and Marks			
Credit	Lecture	Practical	Tutorial	FA		SA	Total
				FA1	FA2		
4	4	-	-	20	20	60	100

Prior Knowledge of:

1. Semiconductor devices and circuits **Is essential**

Course Objectives:

1. Describe ASIC physical design flow for full custom and semi-custom design approach
2. Understand the process involved in semiconductor manufacturing and fabrication.

Course Outcomes: After completion of this course Students should be able to :

1. Understand the ASIC Physical design floor planning and placementalgorithms
2. Explain the full custom and semicustom design concepts in VLSI physical design
3. Express process of clock tree synthesis and it distribution and routing
4. Identify different lithographic process in fabrication technology
5. Explain the processes- etching, oxidation, deposition involved in semiconductor manufacturing.
6. Understand the process flow for CMOS, PMOS , NMOS; and packaging functions and operations.

Detailed Syllabus:

Unit	Description	Duration
1.	ASIC physical design issues, System Partitioning, Floor planning and Placement. Algorithms: K-L-Kernigham-Lin's algorithm, FM- Fiduccia Mattheyes algorithm ,Simulated annealing algorithms.	11
2.	Full Custom Design: Basics, Needs and Applications. Schematic and layout basics, Full Custom Design Flow. Semicustom Approach: Synthesis (RTL to Gate netlist) - Introduction to Constraints (SDC), Introduction to Static Timing Analysis (STA). Place and Route (Logical to Physical Implementation): Floorplan and Power-Plan,	9
3.	Placement, Clock Tree Synthesis- clock planning and distribution, Routing: Timing Optimization, GDS generation	11
4.	IC Technology: Crystal growth, Basic wafer fabrication operations, process yields, Semiconductor material preparation, Basic wafer fabrication operations, Yield measurement; Contamination sources, Clean room construction; Oxidation: dry oxidation, wet oxidation; Lithography. The Photolithographic Process, Photomask Fabrication, Comparison between positive and negative photoresists, Exposure Systems, Characteristics of Exposure Systems, E-beam Lithography, X- ray lithography.	9
5	Etching: Dry etching, Wet etching, resist stripping; Doping: Diffusion process steps, deposition, Drivein oxidation, Ion implantation-1, Ion implantation-2; Deposition: CVD basics, CVD process steps, Low pressure CVD systems, Plasma enhanced CVD systems, Vapour phase epitaxy, molecular beam epitaxy; Chemical mechanical polishing; Metallization.	11
6	Process flow for NMOS, PMOS, CMOS, BICMOS ICs, Novel MOS and GaN based devices. Design rules, stick diagrams and layout.Packaging: Chip characteristics, package functions, package operations	9
Total		60

Text Books:

1. H.Gerez, “Algorithms for VLSI Design Automation”, John Wiley, 1999
2. Sarrafzadeh, M. and Wong, C.K., “An Introduction to VLSI Physical Design”, 4th Ed., McGraw-Hill.
3. S.M. Sze, VLSI technology, Tata McGraw-Hill, Second Edition, 2017. 2. R.C. Jaeger, Introduction to microelectronic fabrication, Prentice Hall, Second Edition, 2013.

Reference Books:

1. Sait, S.M. and Youssef, H., “VLSI Physical Design Automation: Theory and Practice”, World Scientific.
2. Sherwani, N.A., “Algorithm for VLSI Physical Design Automation”, 2nd Ed., Kluwer.
3. Wong, B.P., Mittal, A., Cao Y. and Starr, G., “Nano-CMOS Circuit and Physical Design”, Wiley.
4. Karl Goser, Nanoelectronics and Nanosystems: From Transistors to Molecular and Quantum Devices, Springer 2005.

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Program:	B. Tech. (E&TC) -Honors in Semiconductor Technology			Semester:	VII /VIII
Course:	Project			Code:	BET28HN11/ BET27HN13
	Teaching Scheme (Hrs./Week)		Evaluation Scheme and Marks		
Credit	Lecture	Practical	FA2	TW	OR	Total
4	-	-	-	100	50	150

Prior Knowledge of: Information management, Machine Learning and IoT **is essential.**

Course Objectives:

1. To emphasize on project implementation to realize acquired knowledge and skills using suitable EDA tools.
2. To provide platform to students to demonstrate and effectively communicate their knowledge.

Course Outcomes: After learning the course, the students should be able to:

1. Understand project requirements and appropriate EDA tools for developing the solution.

Detailed Guidelines:

1. Project should be individual and preferably from Industry.
2. The project guidelines mentioned in B.Tech (E&TC) structure will be followed for evaluation of performance and certification compliance.

Vision and Mission of E&TC Department

VISION : To be recognized as a distinguished department in the field of electronics and telecommunication transforming students into competent technocrats by providing an Ethical, Sustainable and Value-Added Quality Education.

MISSION :

1. To create competent Electronics and Tele-communication engineers with Knowledge, Skill and Attitude by establishing a conducive learning environment.
2. To nurture technical competency, entrepreneurship skills and promote higher studies through the state-of-art facilities for building successful careers.
3. To facilitate research by engaging in projects of industrial requirement and national importance.
4. To impart Life skills, Ethical and Social values for self-sustainability.

Programme Educational Objectives (PEO's)

1. Establish a strong base in mathematics, basic sciences, and the fundamental principles of Electronics and Telecommunication Engineering for the students.
2. Equip students with a comprehensive understanding of Electronics and Telecommunication Engineering, enabling them to effectively comprehend, analyse, design, and to innovate practical solutions for real-world challenges.
3. Foster the development of effective communication skills, teamwork, and professional ethics among students, in order to meet the demands of employers and prepare them for higher studies and successful careers.
4. Promote social consciousness and a sense of responsibility among students, creating awareness about their commitment and obligations to society.

Program Outcomes (PO's)

Engineering Graduates will be able to:

1. **Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

2. **Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics,natural sciences, and engineering sciences.
3. **Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
4. **Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
5. **Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
6. **The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
7. **Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
8. **Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
9. **Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
10. **Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
11. **Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply thesssse to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
12. **Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Program Specific Outcomes (PSOs)

1. **PSO1:** Ability to exhibit the competency to solve the problems related to Electronics & Telecommunications Engineering by applying advanced knowledge in the fields of VLSI, Embedded Systems, Signal Processing, Communication, Computing and Automation.
2. **PSO2:** Ability to design and analyse Electronics & Telecommunications systems using state of the art hardware and software tools to address the needs of the industry and society.
3. **PSO3:** Ability to build research and problem-solving attitude through Project based learning to address the societal, environmental, health and safety issues.